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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,665	11/07/2002	Lin-Kai Bu	HMOP0006USA	8010

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P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
NGUYEN, JENNIFER T	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,665	BU ET AL.	
	Examiner	Art Unit	
	Jennifer T Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30-33* is/are allowed.

6)☒ Claim(s) *1-23 and 27-29* is/are rejected.

7)☒ Claim(s) *24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112 second paragraph of 35 U.S.C. 112

A single claim which claims both an apparatus and the method steps of using the apparatus is indefinite under 35 U.S.C. 112, second paragraph. In Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990) and see MPEP 2173.05(p) Section II.

Regarding claim 1, claim 1 combines a method of driving a liquid crystal display device comprising: steps a, b, and c and the LCD device comprising: LCD panel, voltage selection circuit, and a plurality of output buffers. Correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-13, 28, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Akimoto et al. (Patent No.: US 6,756,962).

Regarding claim 1, referring to Fig. 1, Akimoto teaches a method of driving a liquid crystal display (LCD) device, the LCD device comprising: an LCD panel for displaying a plurality of pixels (11) arranged in a matrix format; a voltage selection circuit (3) for outputting a

plurality of driving voltage levels according to display data; and a plurality of output buffers (20), each output buffer electrically connected to the voltage selection circuit and the LCD panel (col. 4, line 34 to col. 5, line 5); the method comprising: driving pixels located in a row by corresponding output buffers according to corresponding driving voltage levels generated from the voltage selection circuit; disconnecting the pixels from the corresponding output buffers; and connecting the pixels driven by the same driving voltage level for equalizing voltages applied on the pixels (col. 5, lines 20-50, col. 10, lines 25-64).

Regarding claim 2, Akimoto teaches turning off operating voltages inputted into the corresponding output buffers after performing step (col. 5, lines 20-50).

Regarding claim 3, Akimoto teaches each output buffer is an operational amplifier (col. 5, lines 51-67).

Regarding claim 4, Akimoto teaches the voltage selection circuit (3) comprises a plurality of conductive wires each for carrying one of the driving voltage levels and a plurality of digital-to-analog decoders (DACs) each for selecting one of the driving voltage levels from the conductive wires according to display data (col. 4, lines 50-67).

Regarding claim 5, Akimoto teaches a plurality of switches each having a first end selectively connected to either an output terminal (16) of the output buffer or an input terminal (17) of the output buffer, and a second end connected to a corresponding pixel (11) (Fig. 1).

Regarding claim 6, Akimoto teaches connecting the first end of the switch in the row to the output terminal of the output buffer (col. 5, lines 20-44).

Regarding claim 7, Akimoto teaches connecting the first end of the switch in the row to the input terminal of the output buffer (col. 5, lines 20-44).

Regarding claim 8, Akimoto teaches the pixels predetermined to be driven to the same driving voltage level are connected to the same conductive wire which delivers corresponding driving voltage level (col. 5, lines 20-44).

Regarding claims 9-12, Akimoto teaches a plurality of first switches (66) each connected between an output terminal of a corresponding output buffer (20) and a corresponding pixel (odd pixel); and a plurality of second switches (67 of upper write circuit and lower write circuit) each connected between two adjacent pixels (odd and even pixel) for selectively connecting the adjacent pixels (Fig. 11).

Regarding claim 13, Akimoto teaches a timing controller (19) for controlling driving (col. 5, lines 1-5).

Regarding claim 28, referring to Figs. 1 and 11, Akimoto teaches a driving device for driving a liquid crystal display (LCD) device, the LCD device comprising an LCD panel having a plurality of pixels arranged in a matrix format, said driving device comprising: a voltage selection module (3) comprising a power supply (1) having a plurality of power transmission lines (2) for carrying a plurality of voltages, and a plurality of decoders each selectively outputting one of the voltages from the power transmission lines according to display data (col. 4, lines 55-57); and a plurality of driving units (16, 17, and 20) each electrically coupled to the one of said decoders, each driving unit comprising an output buffer (20) and a switch (16, 17), a first end of said switch being selectively connected to either an output terminal of said output buffer (i.e., switch 16 connects to output terminal of the output buffer 20) or an input terminal of said output buffer (i.e., switch 17 connects to input terminal of the output buffer 20), a second end of said switch being connected to an output terminal of said driving unit; wherein the first

end of said switch is first connected to the output terminal of said output buffer for driving an output voltage of the driving unit toward a voltage transmitted via one of the power transmission lines of said power supply, and the first end of said switch is then connected to the input terminal of said output buffer for driving the output voltage of said driving unit toward an average voltage generated from averaging voltages at output terminals of said driving units that are connected to the same power transmission line through corresponding decoders (col. 5, lines 20-50, col. 10, lines 25-64).

Regarding claim 29, referring to Fig. 11, Akimoto teaches a driving device for driving a liquid crystal display (LCD) device, the LCD device comprising an LCD panel having a plurality of pixels (11) arranged in a matrix format, said driving device comprising: a plurality of decoders (3) each for selectively outputting one of a plurality of voltages according to display data; a plurality of driving units (66, 67, 20) each electrically connected to one of said decoders, said driving unit comprising: an output buffer (20); a first switch connected between an output terminal of said output buffer and an output terminal of said driving unit, the output terminal of said output buffer being electrically connected to the output terminal of said driving unit when said first switch is turned on (i.e., the switch 66 of upper write circuit connects to pixel 11); and a second switch connected between the output terminal of said driving unit and an output terminal of another driving unit, the output terminal of said driving unit being electrically connected to the output terminal of another driving unit when said second switch is turned on (i.e., the switch 66 of upper write circuit connects to odd pixel and the switch 67 of lower write circuit connects to even pixel); wherein said first switch is first turned on to drive an output voltage of said driving unit toward a voltage from corresponding decoder, and said second switch is then selectively

turned on to drive the output voltage of said driving units toward an average voltage generated from averaging voltages at output terminals of said driving units (col. 5, lines 20-50, col. 10, lines 25-64, and col. 12, lines 25-50).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 14-17, 21-23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto et al. (Patent No.: US 6,756,962) in view of Imamura (Patent No.: 6,466,192).

Regarding claims 14-17, Akimoto differs from claims 14-17 in that he does not specifically teach the timing controller comprises: a frequency divider for dividing the frequency of a clock signal according to a predetermined divisor; a counter for counting the divided clock signal to generate a count value; and a comparator for comparing the count value with a predetermined number to generate a comparison result. However, referring to Fig. 2, Imamura teaches the timing controller comprises: a frequency divider (121) for dividing the frequency of a clock signal according to a predetermined divisor; a counter (122) for counting the divided clock signal to generate a count value; and a comparator (133) for comparing the count value with a predetermined number to generate a comparison result (col. 6, lines 6-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the timing controller as taught by Imamura in the system of Akimoto in order to generate clock signal to control driving of the display panel efficiently.

Regarding claims 21 and 27, Akimoto teaches a liquid crystal display (LCD) device comprising: an LCD panel for displaying a plurality of pixels arranged in a matrix format; a voltage selection circuit (3) for outputting a plurality of driving voltage levels according to display data; a plurality of output buffers (20), each output buffer (20) electrically connected to the voltage selection circuit (3) and the LCD panel for driving the corresponding pixel (11) by corresponding driving voltage level; and a timing controller (19) for controlling driving of the pixels (Fig. 1, col. 4, line 34 to col. 5, line 5); wherein the output buffers are disconnected from the corresponding pixels, and the pixels that are driven by the same driving voltage level are connected for averaging the voltage applied on the pixels (col. 5, lines 20-50, col. 10, lines 25-64).

Akimoto differs from claims 21 and 27 in that he does not specifically teach the timing controller comprising: a frequency divider for dividing the frequency of a clock signal according to a predetermined divisor; a counter for counting the divided clock signal to generate a count value; and a comparator for comparing the count value with a predetermined number; wherein when the count value is equal to the predetermined number. However, referring to Fig. 2, Imamura teaches the timing controller comprises: a frequency divider (121) for dividing the frequency of a clock signal according to a predetermined divisor; a counter (122) for counting the divided clock signal to generate a count value; and a comparator for (133) comparing the count value with a predetermined number; wherein when the count value is equal to the predetermined number (col. 6, lines 6-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the timing controller as

taught by Imamura in the system of Akimoto in order to generate clock signal to control driving of the display panel efficiently.

Regarding claim 21 and 22, the combination of Akimoto and Imamura teaches the frequency divider comprises an input port for receiving an input data to set the predetermined divisor and the comparator comprises an input port for receiving an input data to set the predetermined number (Fig. 2, col. 6, lines 6-15 of Imamura)

7. Claims 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 30-33 are allowed.

9. The prior art made of record and not relied upon is considered to pertinent applicant's disclosure.

Kim et al. (U.S. Patent No. 6,331,847) teaches TFT LCD device that generates gray level voltages having reduced offset margins.

Udo et al. (U.S. Patent No. 6,747,624) teaches driving circuit for supplying tone voltages to LCD.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Jennifer T. Nguyen** whose telephone number is **703-305-3225.** The examiner can normally be reached on Mon-Fri from 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reach at **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to: 703-872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, sixth-floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is 703-306-0377.

JNguyen
12/06/2004

REGINA LIANG
PRIMARY EXAMINER